WHAT IS CLAIMED IS:

1. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, counting the network clock cycles modulo 2^P, where 2^P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period;

(c) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2^P count of network clock cycles at that time;

(d) determining from the RTSs received at the destination node, the number of network clock cycles in each RTS period;

(e) generating a pulse signal from the network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of network clock cycles in the corresponding RTS period; and

(f) multiplying the frequency of the pulse signal generated in step (e) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

2. The method of claim 1 wherein the network clock frequency is less than or equal to twice the service clock frequency.

3. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, dividing the network clock by a rational factor to form a derived network clock;

(c) at the source node, counting the derived network clock cycles modulo 2^P, where 2^P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period;

(d) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

(e) at the destination node dividing the network clock by the same rational factor used at the source node to form a derived network clock equal to the derived network clock at the source node;

(f) determining from the RTSs received at the destination node, the number of derived network clock cycles in each RTS period;

(g) generating a pulse signal from the derived network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of derived network clock cycles in the corresponding RTS period; and

(h) multiplying the frequency of the pulse signal generated in step (g) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

4. The method of claim 3 wherein the derived network clock frequency is less than or equal to twice the service clock frequency.

5. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

counting means connected to the network clock for counting network clock cycles modulo 2^P, where 2^P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the end of each RTS period that is equal to the modulo 2^P count of network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

converting means responsive to the received RTSs and the network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of network clock cycles associated with the counts of network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said dividing means for recovering the timing clock of the service input.

6. Apparatus in accordance with claim 5 wherein the network clock frequency is less than or equal to twice the service clock frequency.

7. Apparatus in accordance with claim 5 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting network clock cycles modulo 2^P;

comparing means for comparing the modulo 2^P count of network clock cycles with a stored RTS and for generating a pulse each time the count of network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of network clock cycles that is greater than a predetermined minimum absolute number of network clock cycles that can occur within any RTS period.

8. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

first dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

second dividing means for dividing the network clock by a rational factor to form a derived network clock;

counting means connected to the network clock for counting derived network clock cycles modulo 2^P, where 2^P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said first dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the

end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

means for dividing the network clock by the same rational factor used at the source node to form a derived network clock;

converting means responsive to the received RTSs and the derived network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of derived network clock cycles associated with the counts of derived network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said first dividing means for recovering the timing clock of the service input.

9. Apparatus in accordance with claim 8 wherein the derived network clock frequency is less than or equal to twice service clock frequency.

10. Apparatus in accordance with claim 8 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting derived network clock cycles modulo 2^P;

comparing means for comparing the modulo 2^P count of derived network clock cycles with a stored RTS and for generating a pulse each time the count of derived network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of derived network clock cycles that is greater than a predetermined minimum absolute number of derived network clock cycles that can occur within any RTS period.

11. Apparatus for generating a representation of the relationship between the timing clock of a service input, at a source node of a packet-based telecommunications network, and a network clock, the apparatus comprising:

(a) means, at the source node, defining a residual time stamp (RTS) period as an integral number N of source-node service clock cycles;

(b) means, at the source node, defining a derived network clock frequency f_{nx} from a network frequency f_n where $f_{nx} = f_n/x$, is a rational number, and f_{nx} is less than or equal to twice the service clock frequency;

(c) means, at the source node, for counting the derived network clock cycles modulo 16 in an RTS period and;

(d) means for transmitting from the source node an RTS that is equal to the modulo 16 count of derived network clock cycles in the RTS period.

12. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of the packet-based telecommunications network, wherein the destination and source nodes have a common network clock or divided network clock and wherein the service node generates a residual time stamp (RTS) signal equal to a modulo 16 count of cycles based on the network clock; the apparatus comprising:

means for receiving the RTS signal;

means for determining the number of network cycles in an RTS period from the RTS signal; and

means responsive to the determining means for generating a clock signal which represents a recovery of the timing clock of the service input.

13. Apparatus for generating a representation of a timing clock of a service input at a source node of a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source node and a destination node; the apparatus comprising:

(a) means for defining a time interval by a fixed number of service clock cycles; and

(b) means for generating a digital representation of a variance of a quantized actual number of network clock cycles within the time interval from an expected number of network clock cycles within the time interval, the variance being within a defined time window which corresponds to a frequency variation of

the source-node service clock and which surrounds the expected number of network clock cycles.

14. The apparatus of claim 13, wherein the digital representation represents a chosen number of the least significant bits of the quantized actual number, the chosen number being sufficient to represent a range of variances based on the source-node service clock variation.

15. The apparatus of claim 14 wherein the chosen number is 4.

16. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said network, wherein a common network clock or divided network clock is provided for the destination node and the source node and a time interval is defined by a fixed number of source-node service clock cycles; the apparatus comprising:

means for receiving a digital representation of a variance of a quantized actual number of network clock cycles from a nominal number of network clock cycles within the time interval, the variance being within a defined time window which corresponds to a source-node service clock variation and which surrounds the nominal number of network clock cycles; and

means for recovering the source-node service clock at the destination node by constructing a timing signal at the destination node based on the variance.

17. Apparatus for reconstructing, at a destination node of a packet-based telecommunications network, a timing clock of a

service input at a source node of the network, wherein a common network clock or divided network clock is provided for the destination node and the source node and wherein the reconstruction is based on successive modulo 2^P numerical representations of the number of network clock cycles within corresponding predetermined time periods, each of the numerical representations being received from the source node and being less than the actual number of network clock cycles within its corresponding time period; the apparatus comprising:

means for receiving the numerical representations in succession at the destination node;

means for converting the received numerical representations into successive fixed time intervals, wherein each successive interval corresponds to the number of network clock cycles in a corresponding one of the predetermined time periods; and

means for recovering the source-node service clock from the fixed time intervals.

18. The apparatus of claim 17, wherein the converting means further comprises:

means for sequentially storing the successive modulo 2^P numerical representations;

means for comparing the successive numerical representations with a modulo 2^P count of the network clock cycles at the destination node to generate a comparison signal for each match between the numerical representation and the modulo 2^P count at the destination node; and

means for successively selecting from the comparison signal the numerical representations occurring after a predetermined minimum number of network clock cycles which can occur within any of the predetermined time periods, wherein the successive selected numerical representations define the successive fixed time intervals.

19. A method for generating a signal at a source node for use in recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes; the steps of the method comprising:

defining a time interval by a fixed number of cycles of the source-node service clock;

determining an actual number of cycles of the network clock within the time interval;

determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval; and

generating a digital signal representing the numerical deviation for transmission through the network to the destination node.

20. A method for recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes, wherein a time interval is defined by a fixed number of cycles of the source-node service clock, and wherein an actual number of cycles of the

network clock within the time interval and a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval are determined; the steps of the method comprising:

receiving a digital signal representing the numerical deviation transmitted through the network from the source node; and

generating a timing signal corresponding to the source-node service clock on the basis of the digital signal representing the numerical deviation.

21. A method for recovering, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the destination node and the source node; the steps of the method comprising:

defining a time interval by a fixed number of cycles of the source-node service clock;

determining an actual number of cycles of the network clock within the time interval;

determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval;

generating a digital signal representing the numerical deviation;

transmitting the digital signal to the destination node; and

generating a timing signal at the destination node corresponding to the source node service clock on the basis of the digital signal and a signal from the network clock.

22. The method of claim 21 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

23. The method of claim 21 further including the step of employing a modulo 2^P counter to generate the numerical deviation.

24. Apparatus for generating a signal at a source node for use in recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes; the apparatus comprising:

means for defining a time interval by a fixed number of cycles of the source-node service clock;

means for determining an actual number of cycles of the network clock within the time interval;

means for determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval; and

means for generating a digital signal representing the numerical deviation for transmission through the network to the destination node.

25. The apparatus of claim 24 wherein the numerical deviation is determined as a function of the fixed number of

source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

26. The apparatus of claim 24 wherein the numerical deviation determining means includes a modulo 2^P counter which generates the numerical deviation.

27. The apparatus of claim 26 wherein a value of 2^P is 16.

28. Apparatus for recovering a source-node clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes and wherein a time interval is defined by a fixed number of cycles of the source-node service clock, and wherein an actual number of cycles of the network clock within the time interval and a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval are determined; the apparatus comprising:

means for receiving a digital signal representing the numerical deviation transmitted through the network from the source node; and

means for generating a timing signal corresponding to the source-node service clock on the basis of the digital signal representing the numerical deviation.

29. Apparatus for recovering, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the packet-based telecommunications network, wherein a common network clock or

divided network clock is provided for the destination node and the source node; the apparatus comprising:

means for defining a time interval by a fixed number of cycles of the source-node service clock;

means for determining an actual number of cycles of the network clock within the time interval;

means for determining a numerical deviation of the actual number of network clock cycles from another number of network clock cycles known nominally to be within the time interval;

means for generating a digital signal representing the numerical deviation;

means for transmitting the digital signal to the destination node; and

means for generating a timing signal at the destination node corresponding to the source-node service clock on the basis of the digital signal and a signal from the network clock.

30. The apparatus of claim 29 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

31. The apparatus of claim 29 wherein the numerical deviation determining means includes a modulo 2^P counter which generates the numerical deviation.

32. The apparatus of claim 29 wherein means are provided for carrying any fractional network cycle in any time interval for

network cycle counting by the modulo 2^P counter for counting the next time interval.

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